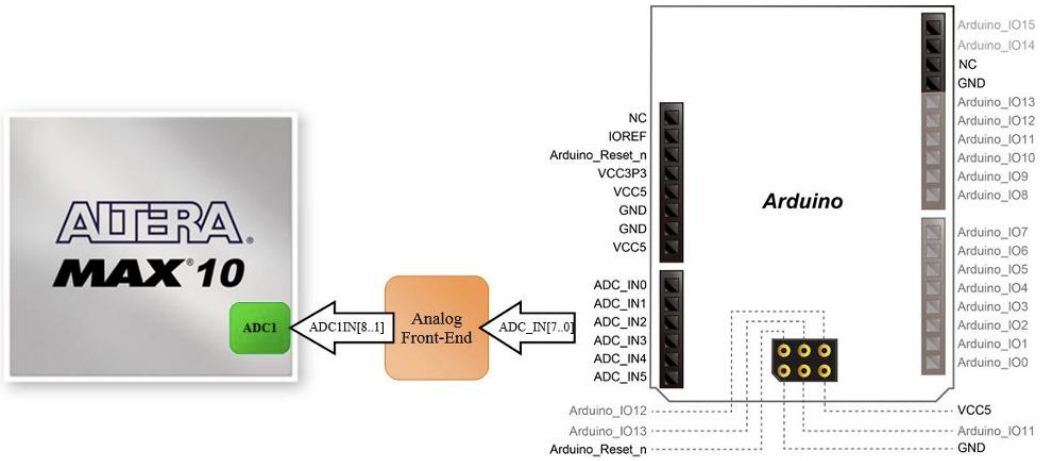
קריאה ממיר ADC של כרטיס DE10lite

ללוח DE10-Lite יש שמונה כניסות אנלוגיות המחוברות ל-ADC1 של MAX 10 FPGA

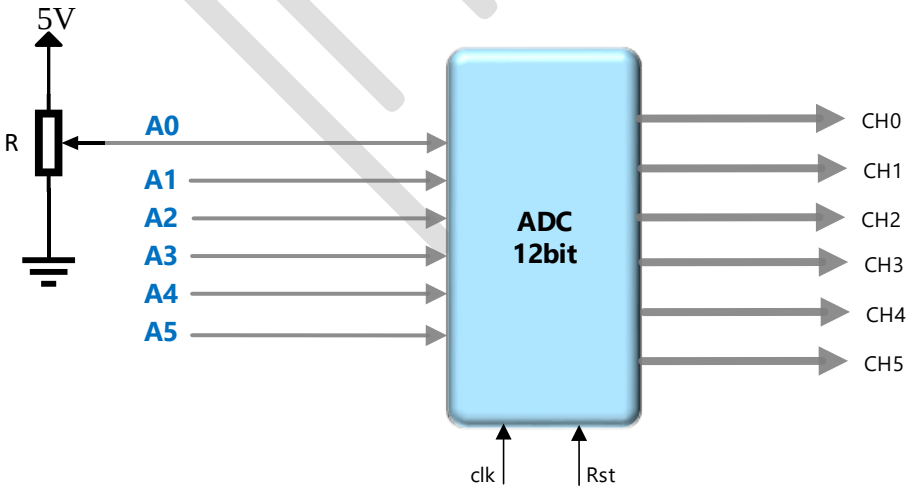
6 כניסות A0 - A5 דרך מחבר JP8.

המתח המרבי בכל כניסה אנלוגית במחבר מותאם ל-5V (מתח הכניסה עובר דרך מעגל פנימי המוריד למתח כניסה מרבי של 2.5V)



Connections between the Arduino Analog input and MAX 10 FPGA

תיאור סכמתי של הממיר



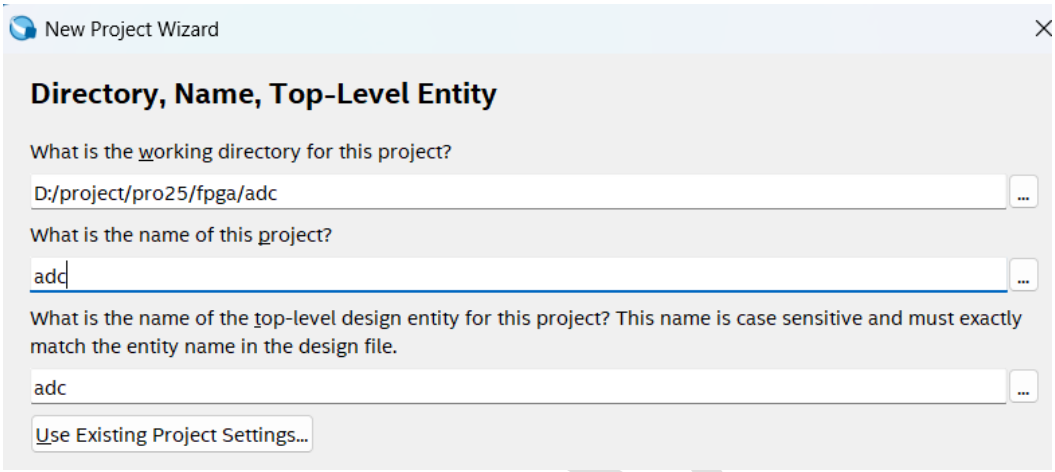
לממיר כניסת clk הקובע את זמן ההמרה ו- Rst הפעיל בגבוה

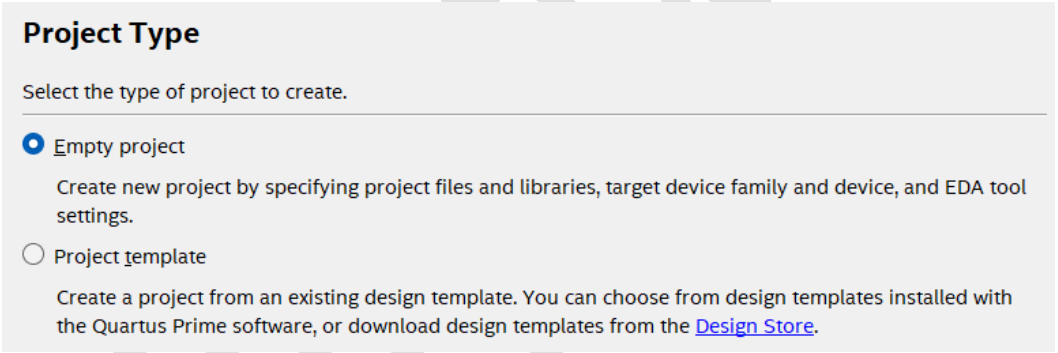
ערך המוצא הדיגיטלי ניתן לחישוב על פי הנוסחה הבאה:

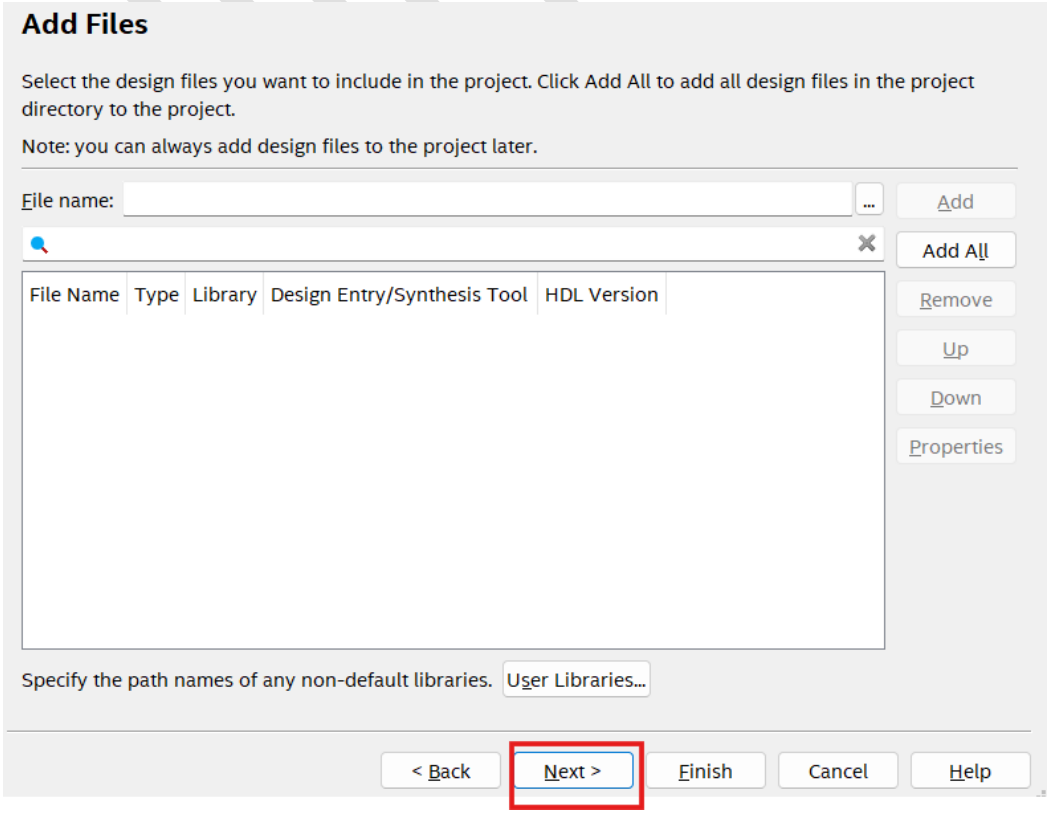
$$DataOut = \frac{V_{in}}{5/2^{12}}$$

שלבים בשילוב הממיר

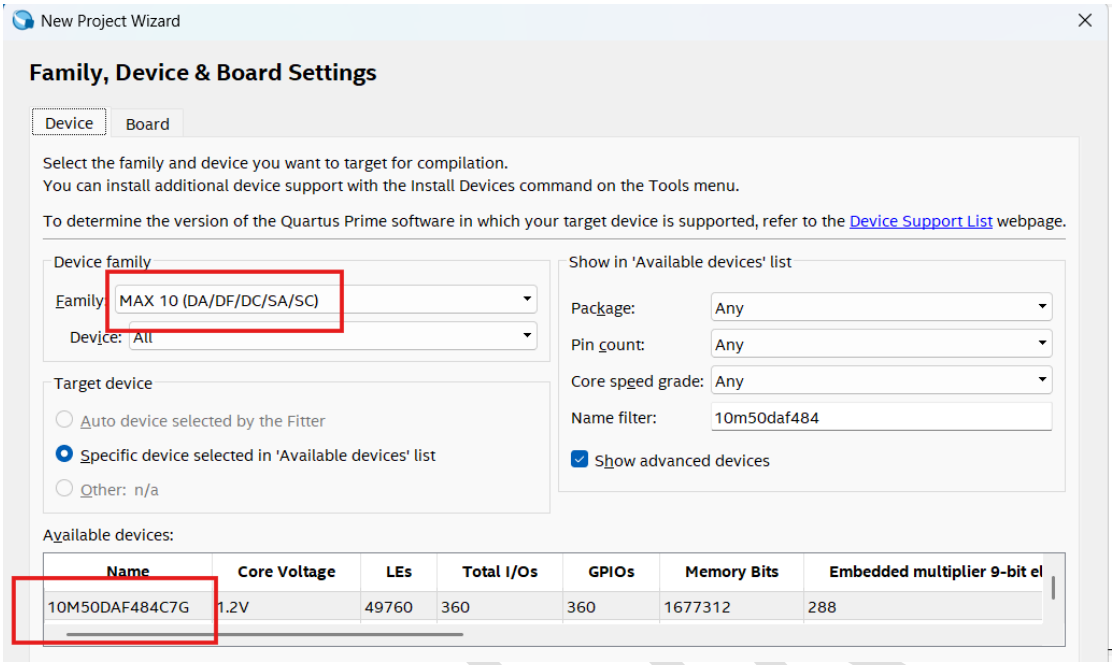
פתיחת פרויקט





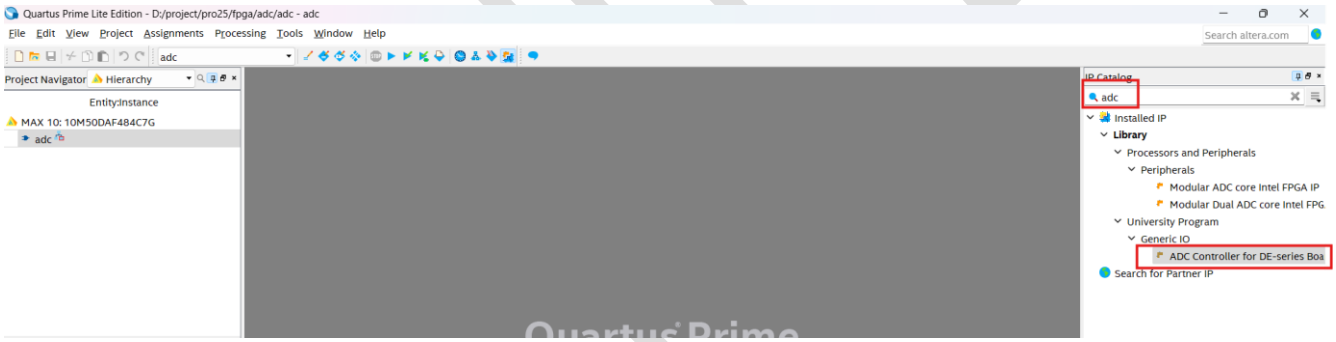


בחירת רכיב

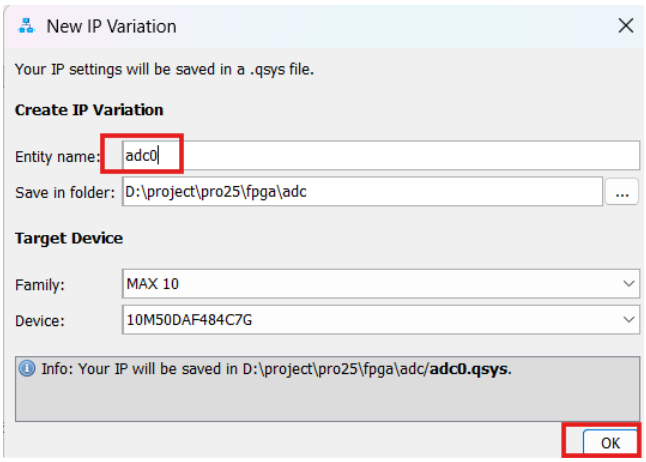


ניכנס ל – Platform Designer

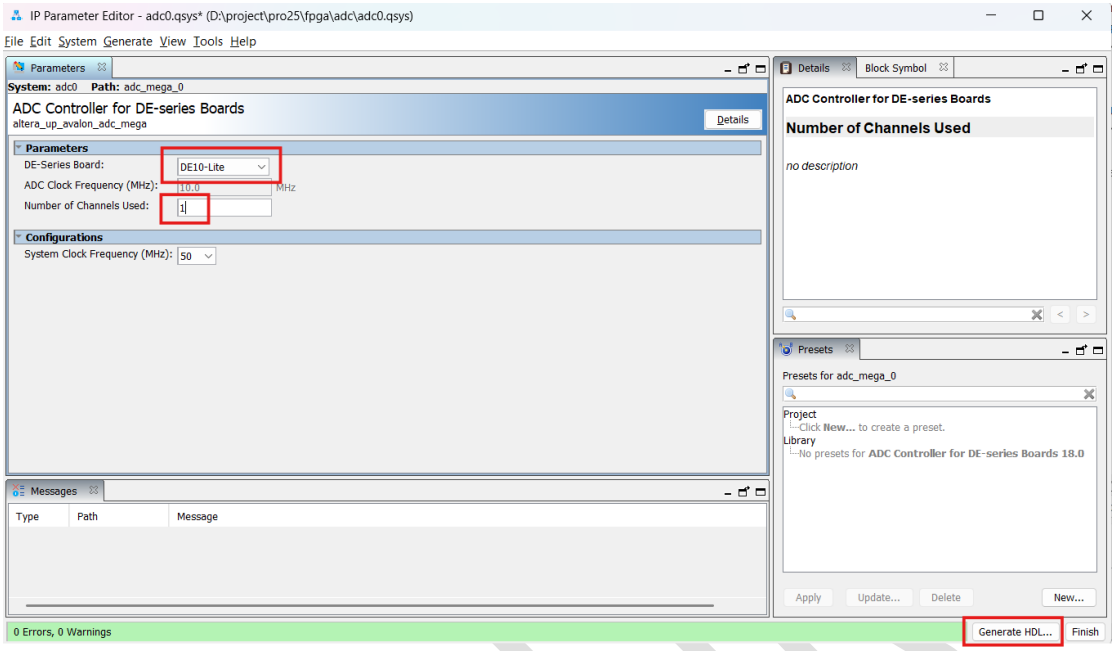
ונבחר את ממיר ה-ADC



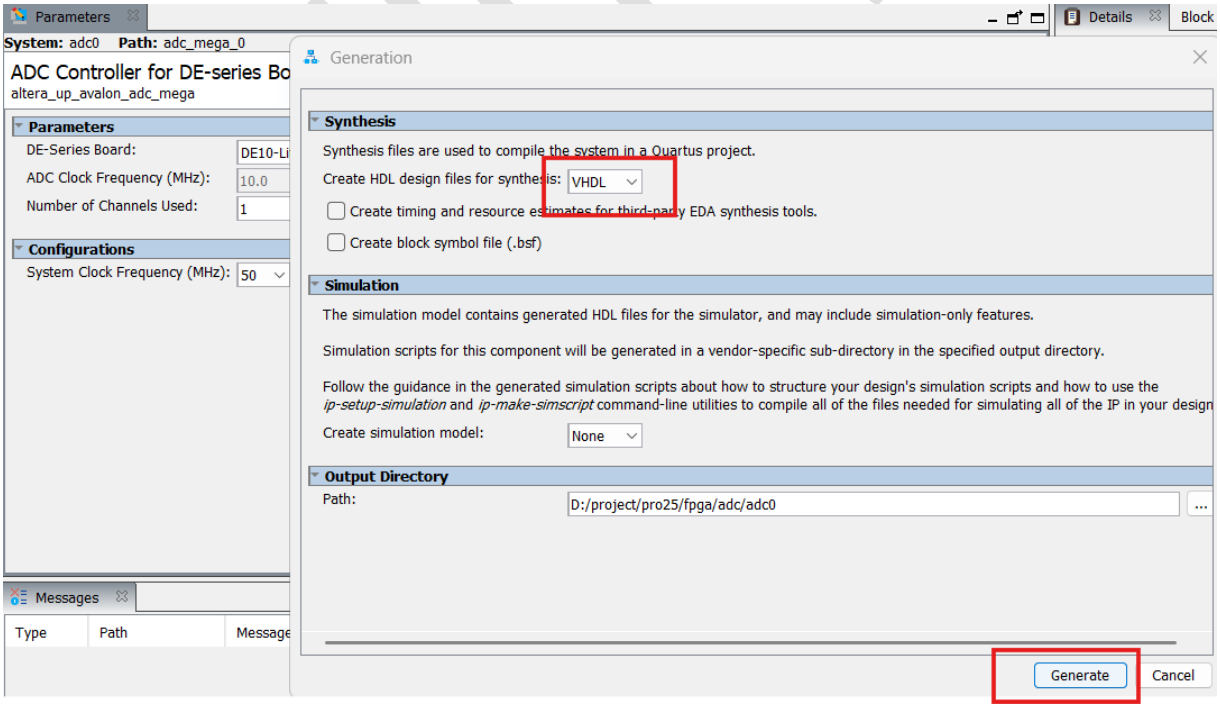
נבחר שם

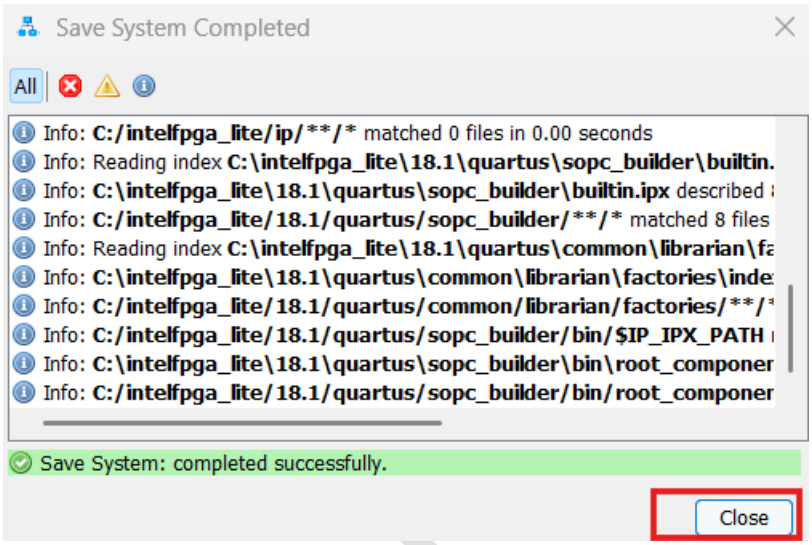


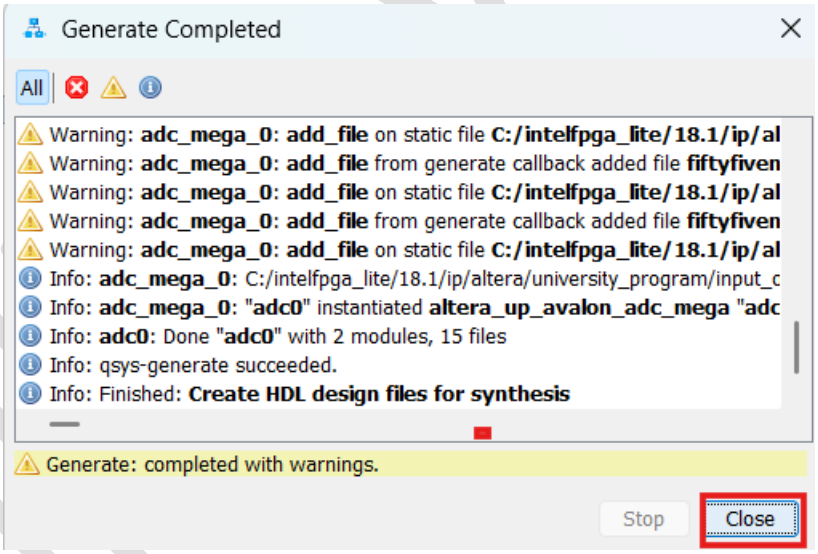
נבחר DE10-Lite ו– Channel אחד עם תדר מקור של 50MHz (של הרכיב , הממיר מקבל תדר נמוך יותר של 10MHz)

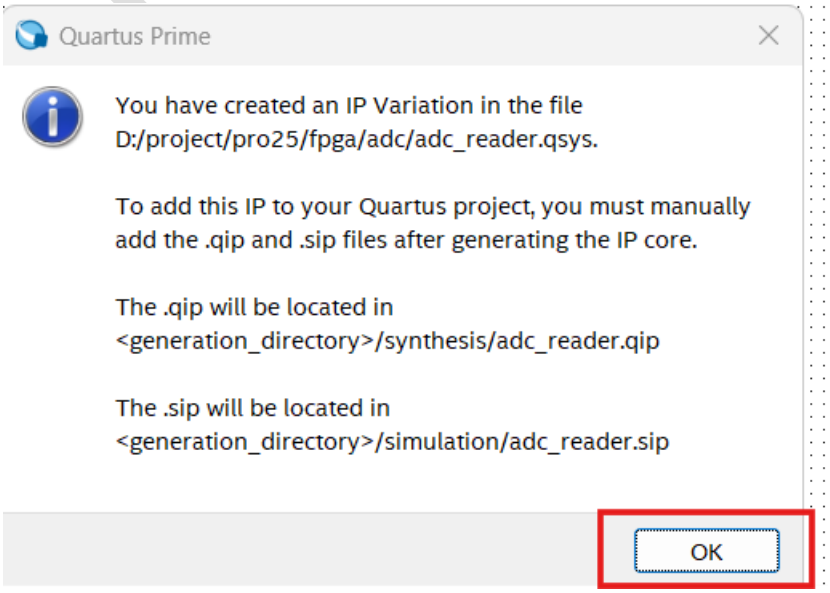


נבחר את השפה של הרכיב

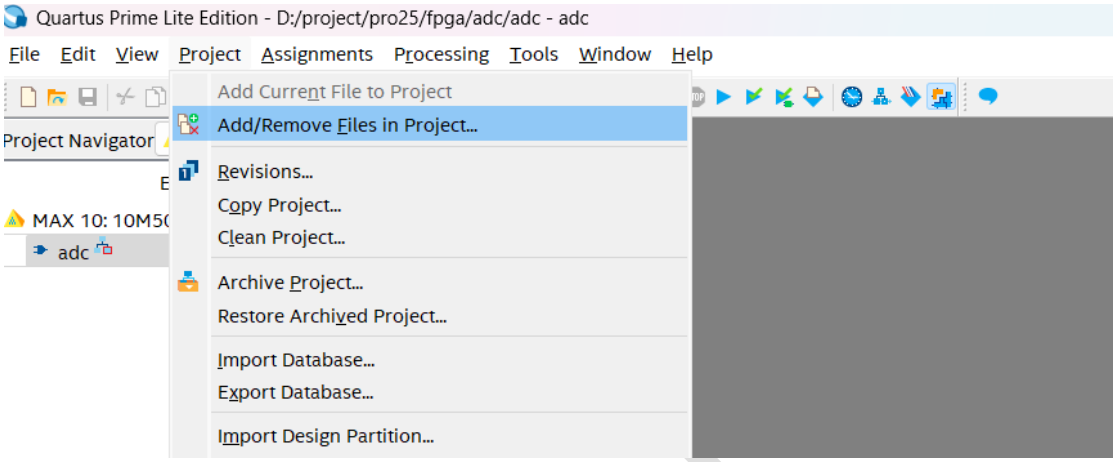



Save System Completed
All
Info: C:/intelfpga_lite/ip/**/* matched 0 files in 0.00 seconds
Info: Reading index C:\intelfpga_lite\18.1\quartus\sopc_builder\builtin.
Info: C:\intelfpga_lite\18.1\quartus\sopc_builder\builtin.ipx described
Info: C:/intelfpga_lite/18.1/quartus/sopc_builder/**/* matched 8 files
Info: Reading index C:\intelfpga_lite\18.1\quartus\common\librarian\fa
Info: C:\intelfpga_lite\18.1\quartus\common\librarian\factories\inde
Info: C:/intelfpga_lite/18.1/quartus/common/librarian/factories/**/
Info: C:/intelfpga_lite/18.1/quartus/sopc_builder/bin/$IP_IPX_PATH
Info: C:\intelfpga_lite\18.1\quartus\sopc_builder\bin\root_componer
Info: C:/intelfpga_lite/18.1/quartus/sopc_builder/bin/root_componer
Save System: completed successfully.
Close

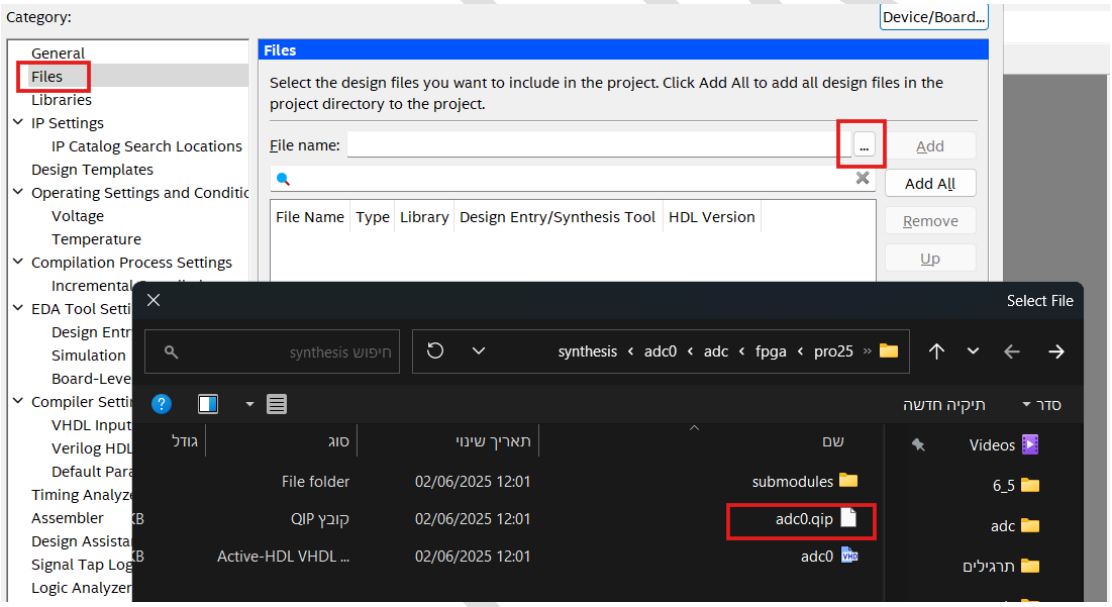

Generate Completed
All
Warning: adc_mega_0: add_file on static file C:/intelfpga_lite/18.1/ip/al
Warning: adc_mega_0: add_file from generate callback added file fiftyfiven
Warning: adc_mega_0: add_file on static file C:/intelfpga_lite/18.1/ip/al
Warning: adc_mega_0: add_file from generate callback added file fiftyfiven
Warning: adc_mega_0: add_file on static file C:/intelfpga_lite/18.1/ip/al
Info: adc_mega_0: C:/intelfpga_lite/18.1/ip/altera/university_program/input_c
Info: adc_mega_0: "adc0" instantiated altera_up_avalon_adc_mega "adc
Info: adc0: Done "adc0" with 2 modules, 15 files
Info: qsys-generate succeeded.
Info: Finished: Create HDL design files for synthesis
Generate: completed with warnings.
Stop
Close


Quartus Prime
You have created an IP Variation in the file
D:/project/pro25/fpga/adc/adc_reader.qsys.
To add this IP to your Quartus project, you must manually
add the .qip and .sip files after generating the IP core.
The .qip will be located in
<generation_directory>/synthesis/adc_reader.qip
The .sip will be located in
<generation_directory>/simulation/adc_reader.sip
OK

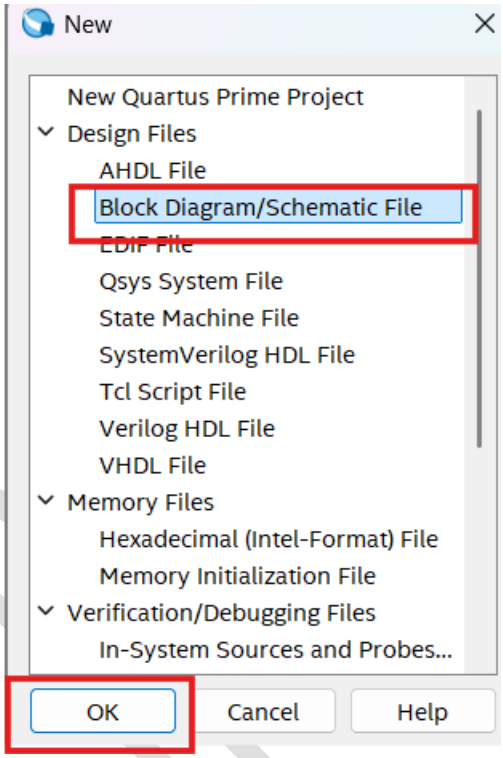
לחזור ל -QUARTUS

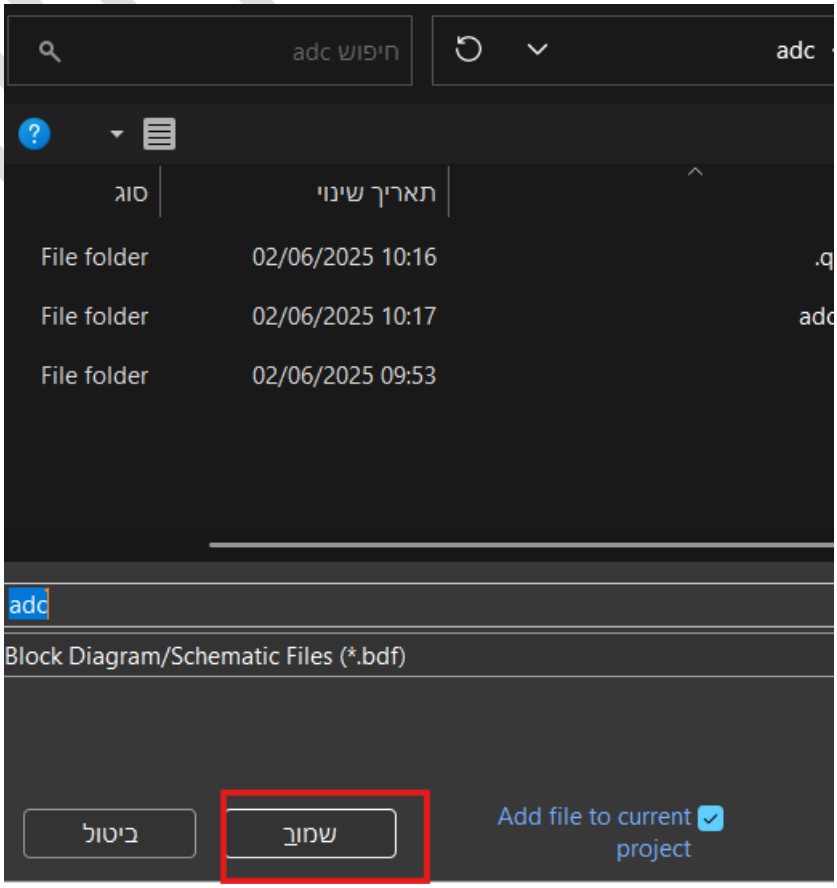


להוסיף קובץ רכיב ה- ADC שנוצר לפרויקט

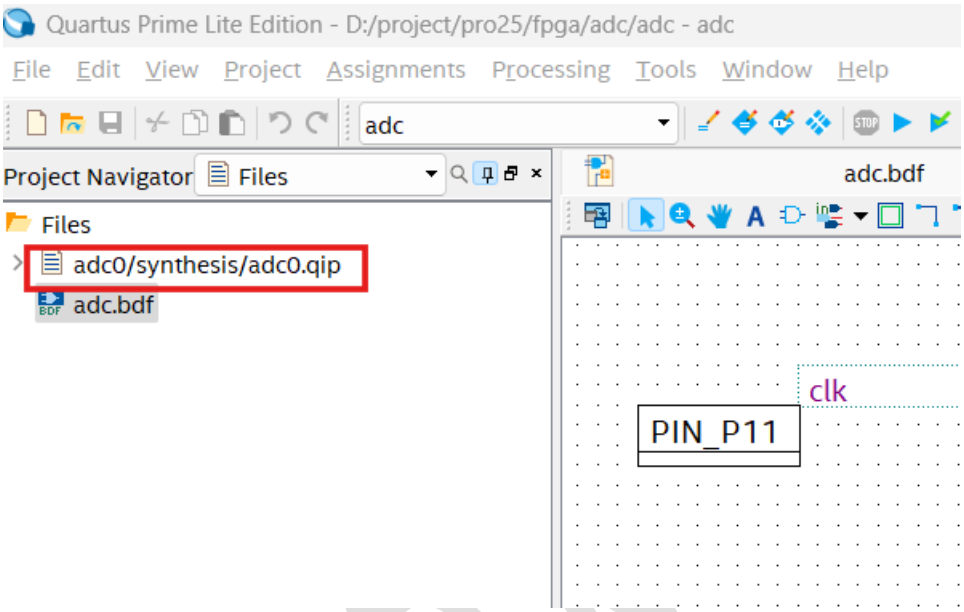


נפתח קובץ Block Diagram

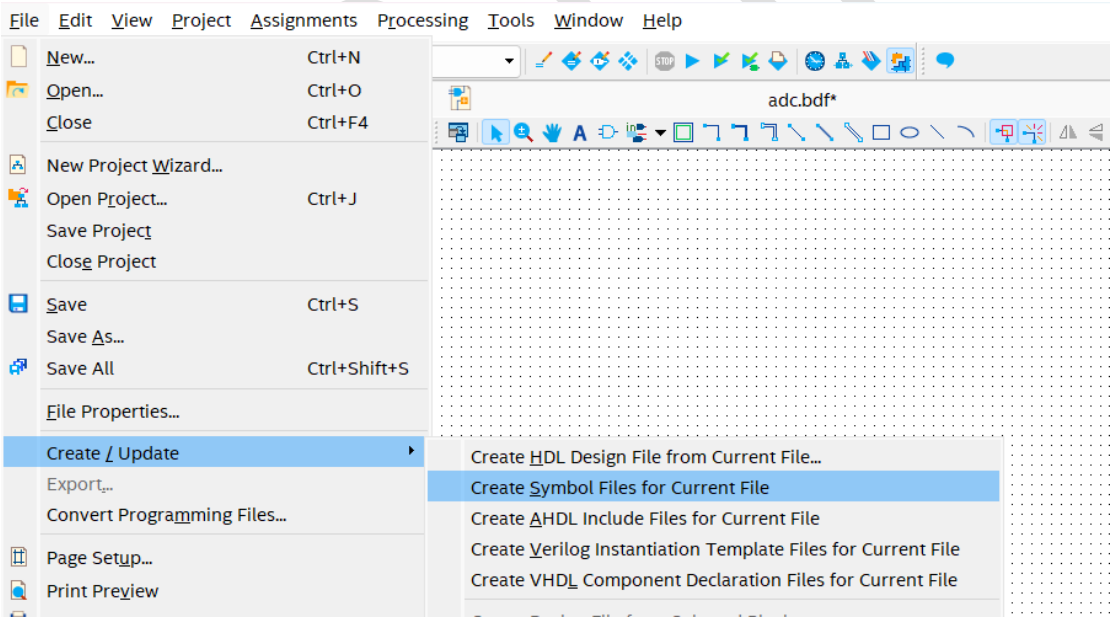




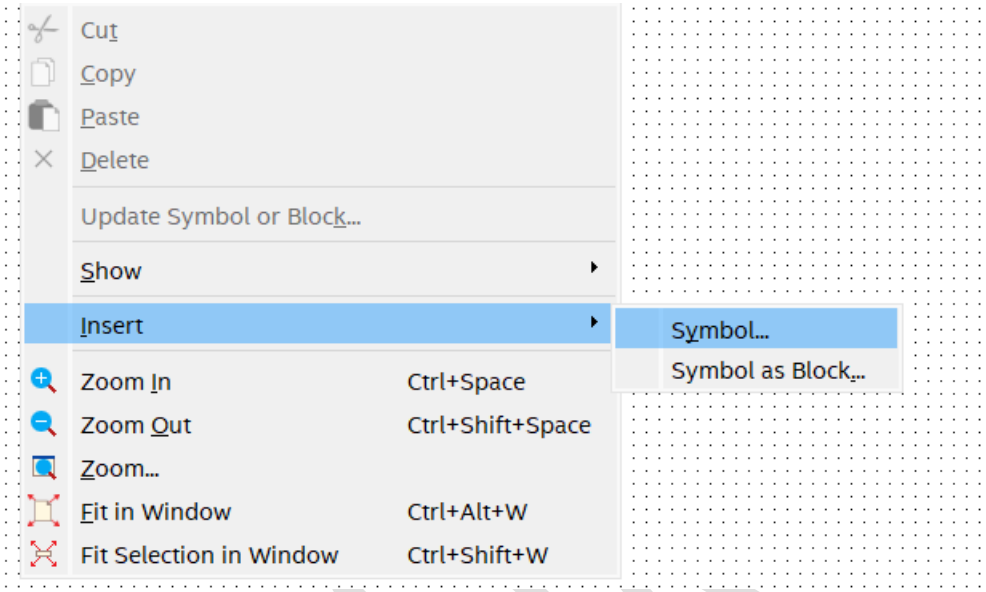
לסמן כדי ליצור Symbol

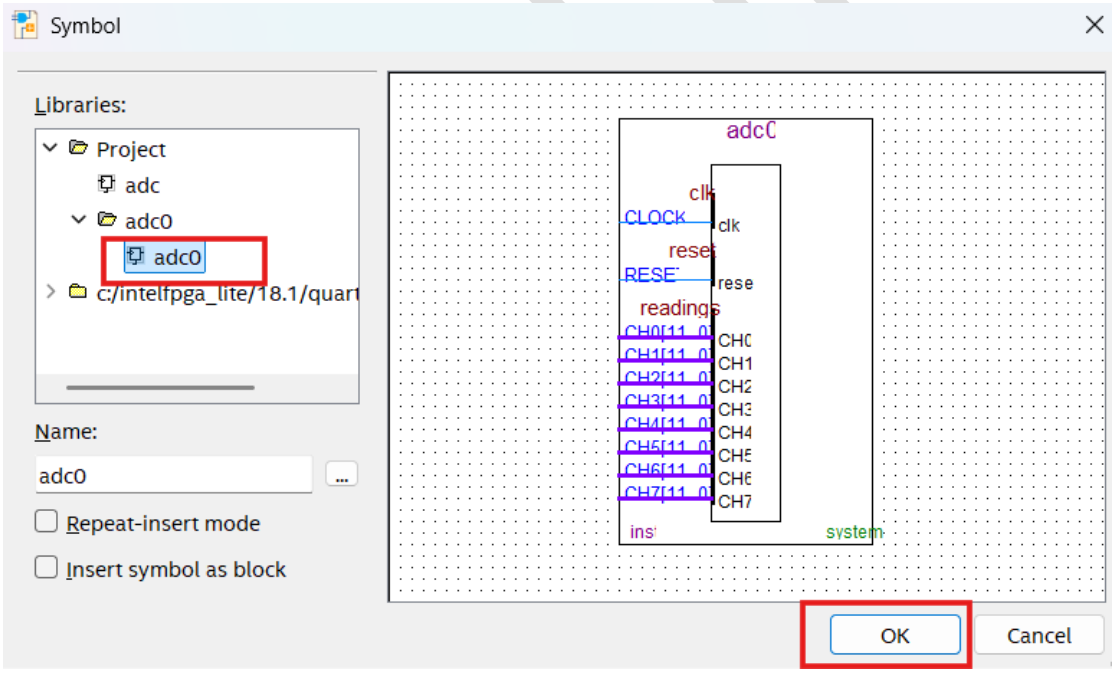


ליצור Symbol



נוסיף בסכימת הבלוקים את הרכיב



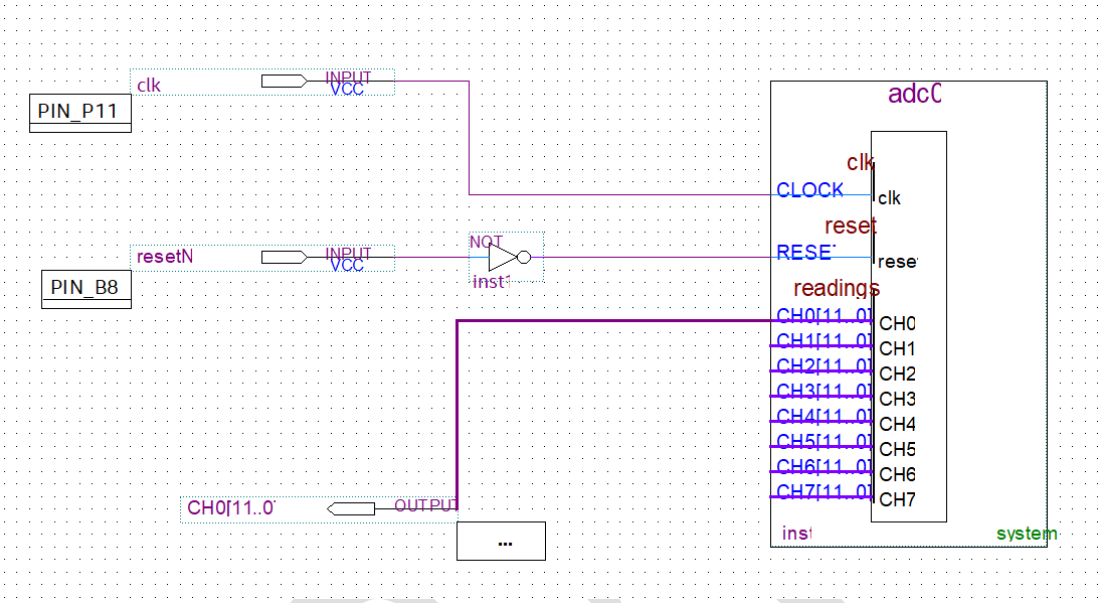


חיבורים

נחבר הדק clk של 50MHz

נחבר את כניסת ה-Reset (פעיל בגבוה) דרך מהפך ללחצן חיצוני הפעיל בנמוך.

מוצא הממיר נחבר ל-10 לדים מתוך 12 הסיביות של הממיר (MSB 10)



נגדיר פינים ל -10 לדים מתוך 12 (MSB)

Named: * Edit:

Node Name	Direction	Location	I/O Bank	VREF Group	itter Locatior	I/O Standard	Reserved	urrent Streng	Slew Rate	ifferential Pai	ict Preservati
CH0[11]	Output	PIN_B11	7	B7_N0	PIN_B11	3.3-V LVTTL		8mA (default)	2 (default)		
CH0[10]	Output	PIN_A11	7	B7_N0	PIN_A11	3.3-V LVTTL		8mA (default)	2 (default)		
CH0[9]	Output	PIN_D14	7	B7_N0	PIN_D14	3.3-V LVTTL		8mA (default)	2 (default)		
CH0[8]	Output	PIN_E14	7	B7_N0	PIN_E14	3.3-V LVTTL		8mA (default)	2 (default)		
CH0[7]	Output	PIN_C13	7	B7_N0	PIN_C13	3.3-V LVTTL		8mA (default)	2 (default)		
CH0[6]	Output	PIN_D13	7	B7_N0	PIN_D13	3.3-V LVTTL		8mA (default)	2 (default)		
CH0[5]	Output	PIN_B10	7	B7_N0	PIN_B10	3.3-V LVTTL		8mA (default)	2 (default)		
CH0[4]	Output	PIN_A10	7	B7_N0	PIN_A10	3.3-V LVTTL		8mA (default)	2 (default)		
CH0[3]	Output	PIN_A9	7	B7_N0	PIN_A9	3.3-V LVTTL		8mA (default)	2 (default)		
CH0[2]	Output	PIN_A8	7	B7_N0	PIN_A8	3.3-V LVTTL		8mA (default)	2 (default)		
CH0[1]	Output				PIN_A12	3.3-V LVTTL		8mA (default)	2 (default)		
CH0[0]	Output				PIN_H13	3.3-V LVTTL		8mA (default)	2 (default)		
clk	Input	PIN_P11	3	B3_N0	PIN_P11	3.3-V LVTTL		8mA (default)			
resetN	Input	PIN_B8	7	B7_N0	PIN_B8	3.3 V ...rigger		8mA (default)			
<<new node>>											

ונצרוב

חיבור תצוגת 7segment של 4 ספרות (0 עד 4095)

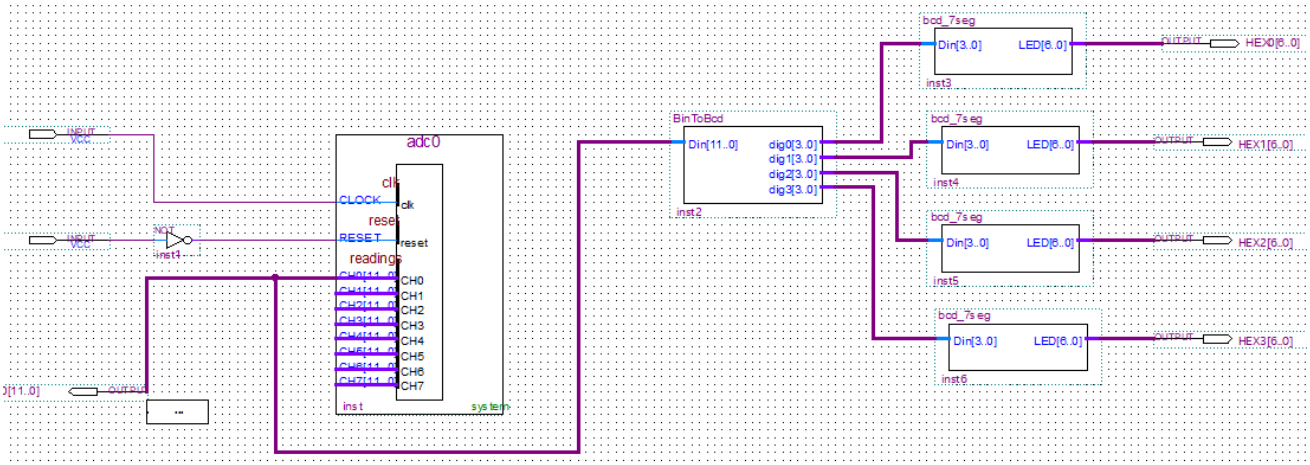
נוסיף קובץ VHDL של מפענח תצוגת 7 segment

```
library IEEE;
use IEEE.std_logic_1164.all;

entity bcd_7seg is
    port(LED: out STD_LOGIC_VECTOR (6 downto 0);
         Din: in std_logic_vector(3 downto 0));
end;
architecture arc_7seg of bcd_7seg is

begin

    -- segment encoding
    --      0
    --     ---
    -- 5 |   | 1
    --     ---  <- 6
    -- 4 |   | 2
    --     ---
    --      3

    with Din select
    LED <=
    "1111001" when "0001", --1
    "0100100" when "0010", --2
    "0110000" when "0011", --3
    "0011001" when "0100", --4
    "0010010" when "0101", --5
    "0000010" when "0110", --6
    "1111000" when "0111", --7
    "0000000" when "1000", --8
    "0010000" when "1001", --9
    "0001000" when "1010", --A
    "0000011" when "1011", --b
    "1000110" when "1100", --C
    "0100001" when "1101", --d
    "0000110" when "1110", --E
    "0001110" when "1111", --F
    "1000000" when others; --0

end;
```

וקובץ המרה מבינארי לקוד BCD

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;
use IEEE.std_logic_arith.all;

entity BinToBcd is
    port(Din: in std_logic_vector(11 downto 0);-- 0 to 999
        dig0,dig1,dig2,dig3: out std_logic_vector(3 downto 0));
end;

architecture arc_BinToBcd of BinToBcd is
begin

    process(Din)

        variable temp : integer range 0 to 4095;
        variable dig0_int,dig1_int,dig2_int,dig3_int :integer range 0
to 9;
    begin
        temp:= conv_integer(Din);
        dig0_int:=temp mod 10;
        dig1_int:=(temp/10) mod 10;
        dig2_int:=(temp/100) mod 10;
        dig3_int:=temp/1000;

        dig0<= conv_std_logic_vector(dig0_int,4);
        dig1<= conv_std_logic_vector(dig1_int,4);
        dig2<= conv_std_logic_vector(dig2_int,4);
        dig3<= conv_std_logic_vector(dig3_int,4);

    end process;
end;
```

בגרפי נחבר לפי השרטוט הבא:



נגדיר פינים

clk	Input	PIN_P11	3	B3_N0	PIN_P11	3.3-V LVTTL		8mA (default)	
HEX0[6]	Output	PIN_C17	7	B7_N0	PIN_C17	3.3-V LVTTL		8mA (default)	2 (default)
HEX0[5]	Output	PIN_D17	7	B7_N0	PIN_D17	3.3-V LVTTL		8mA (default)	2 (default)
HEX0[4]	Output	PIN_E16	7	B7_N0	PIN_E16	3.3-V LVTTL		8mA (default)	2 (default)
HEX0[3]	Output	PIN_C16	7	B7_N0	PIN_C16	3.3-V LVTTL		8mA (default)	2 (default)
HEX0[2]	Output	PIN_C15	7	B7_N0	PIN_C15	3.3-V LVTTL		8mA (default)	2 (default)
HEX0[1]	Output	PIN_E15	7	B7_N0	PIN_E15	3.3-V LVTTL		8mA (default)	2 (default)
HEX0[0]	Output	PIN_C14	7	B7_N0	PIN_C14	3.3-V LVTTL		8mA (default)	2 (default)
HEX1[6]	Output	PIN_B17	7	B7_N0	PIN_B17	3.3-V LVTTL		8mA (default)	2 (default)
HEX1[5]	Output	PIN_A18	7	B7_N0	PIN_A18	3.3-V LVTTL		8mA (default)	2 (default)
HEX1[4]	Output	PIN_A17	7	B7_N0	PIN_A17	3.3-V LVTTL		8mA (default)	2 (default)
HEX1[3]	Output	PIN_B16	7	B7_N0	PIN_B16	3.3-V LVTTL		8mA (default)	2 (default)
HEX1[2]	Output	PIN_E18	6	B6_N0	PIN_E18	3.3-V LVTTL		8mA (default)	2 (default)
HEX1[1]	Output	PIN_D18	6	B6_N0	PIN_D18	3.3-V LVTTL		8mA (default)	2 (default)
HEX1[0]	Output	PIN_C18	7	B7_N0	PIN_C18	3.3-V LVTTL		8mA (default)	2 (default)
HEX2[6]	Output	PIN_B22	6	B6_N0	PIN_B22	3.3-V LVTTL		8mA (default)	2 (default)
HEX2[5]	Output	PIN_C22	6	B6_N0	PIN_C22	3.3-V LVTTL		8mA (default)	2 (default)
HEX2[4]	Output	PIN_B21	6	B6_N0	PIN_B21	3.3-V LVTTL		8mA (default)	2 (default)
HEX2[3]	Output	PIN_A21	6	B6_N0	PIN_A21	3.3-V LVTTL		8mA (default)	2 (default)
HEX2[2]	Output	PIN_B19	7	B7_N0	PIN_B19	3.3-V LVTTL		8mA (default)	2 (default)
HEX2[1]	Output	PIN_A20	7	B7_N0	PIN_A20	3.3-V LVTTL		8mA (default)	2 (default)
HEX2[0]	Output	PIN_B20	6	B6_N0	PIN_B20	3.3-V LVTTL		8mA (default)	2 (default)
HEX3[6]	Output	PIN_E17	6	B6_N0	PIN_E17	3.3-V LVTTL		8mA (default)	2 (default)
HEX3[5]	Output	PIN_D19	6	B6_N0	PIN_D19	3.3-V LVTTL		8mA (default)	2 (default)
HEX3[4]	Output	PIN_C20	6	B6_N0	PIN_C20	3.3-V LVTTL		8mA (default)	2 (default)
HEX3[3]	Output	PIN_C19	7	B7_N0	PIN_C19	3.3-V LVTTL		8mA (default)	2 (default)
HEX3[2]	Output	PIN_E21	6	B6_N0	PIN_E21	3.3-V LVTTL		8mA (default)	2 (default)
HEX3[1]	Output	PIN_E22	6	B6_N0	PIN_E22	3.3-V LVTTL		8mA (default)	2 (default)
HEX3[0]	Output	PIN_F21	6	B6_N0	PIN_F21	3.3-V LVTTL		8mA (default)	2 (default)
resetN	Input	PIN_B8	7	B7_N0	PIN_B8	3.3 V Sc... Trigger		8mA (default)	

ונצרוב