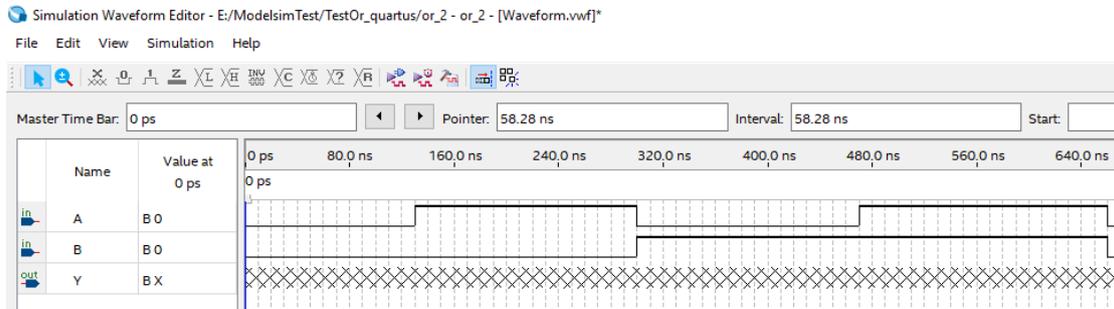


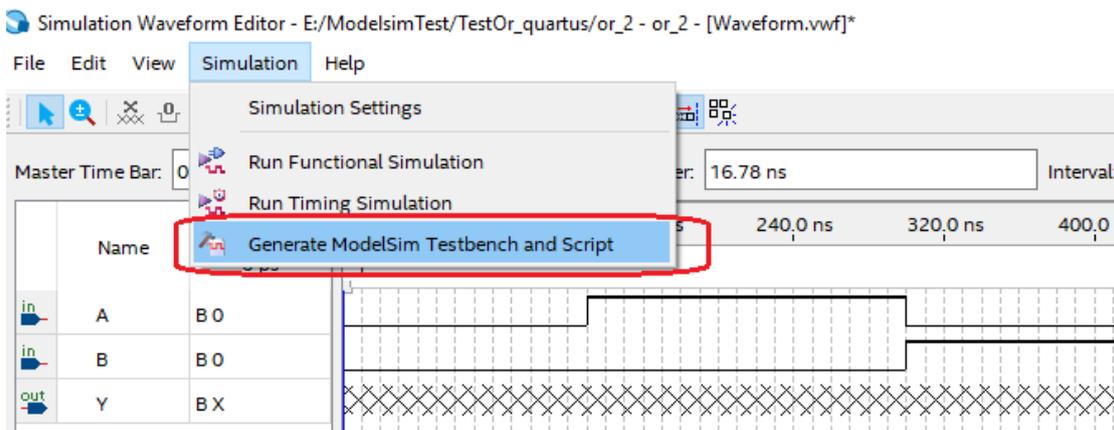
יצירת Testbench מתוך QUARTUS

- לאחר בדיקה והרצה ב-QUARTUS
- סימולציה

נסמן את המצבים הלוגיים בתרשים הסימולציה



- נסמן יצירת Testbench



התוכנה יצרה קובץ Testbench - Waveform.vwf.vht

בתיקה : \simulation\modelsim

```
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```

```

--
*****
*****
-- This file contains a Vhdl test bench with test vectors .The test
vectors
-- are exported from a vector file in the Quartus Waveform Editor and
apply to
-- the top level entity of the current Quartus project .The user can
use this
-- testbench to simulate his design using a third-party simulation
tool .
--
*****
*****
-- Generated on "01/18/2020 17:45:07"

-- Vhdl Test Bench(with test vectors) for design      :      or_2
--
-- Simulation tool : 3rd Party
--

LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY or_2_vhd_vec_tst IS
END or_2_vhd_vec_tst;
ARCHITECTURE or_2_arch OF or_2_vhd_vec_tst IS
-- constants
-- signals
SIGNAL A : STD_LOGIC;
SIGNAL B : STD_LOGIC;
SIGNAL Y : STD_LOGIC;
COMPONENT or_2
    PORT (
        A : IN STD_LOGIC;
        B : IN STD_LOGIC;
        Y : OUT STD_LOGIC
    );
END COMPONENT;
BEGIN
    i1 : or_2
        PORT MAP (
-- list connections between master ports and signals
        A => A,
        B => B,
        Y => Y
        );

-- A
t_prcs_A: PROCESS
BEGIN
    A <= '0';
    WAIT FOR 130000 ps;
    A <= '1';
    WAIT FOR 170000 ps;
    A <= '0';
    WAIT FOR 170000 ps;
    A <= '1';
    WAIT FOR 190000 ps;
    A <= '0';
WAIT;

```

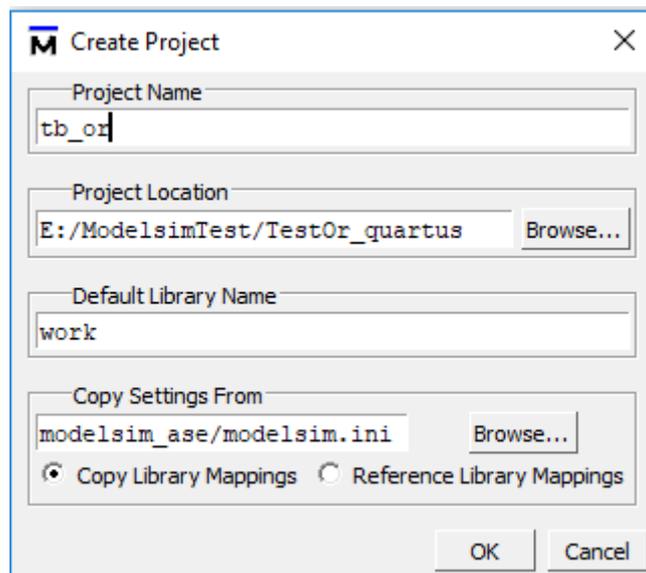
```

END PROCESS t_prs_A;

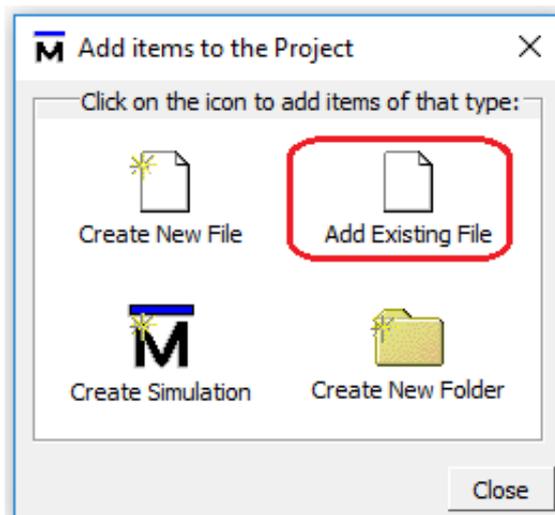
-- B
t_prs_B: PROCESS
BEGIN
    B <= '0';
    WAIT FOR 300000 ps;
    B <= '1';
    WAIT FOR 360000 ps;
    B <= '0';
WAIT;
END PROCESS t_prs_B;
END or_2_arch;

```

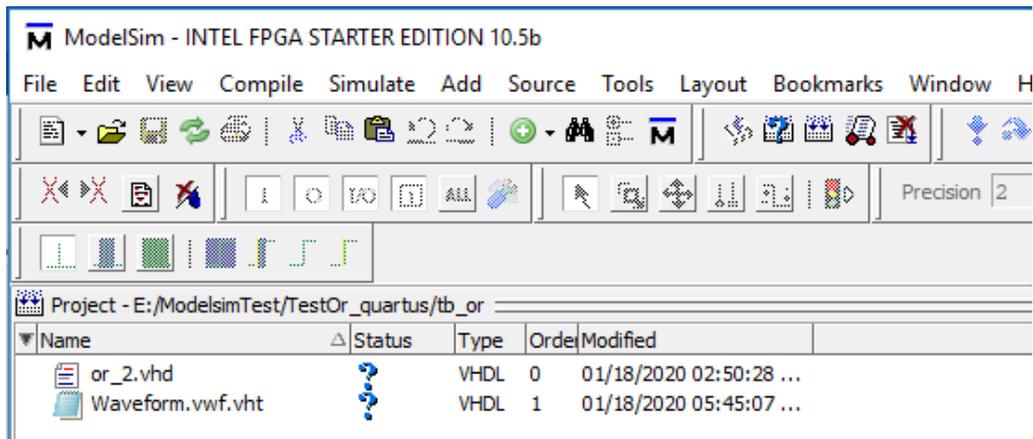
- נפתח פרויקט חדש



- נוסף את שני קבצים מתוך הספריות המתאימות:



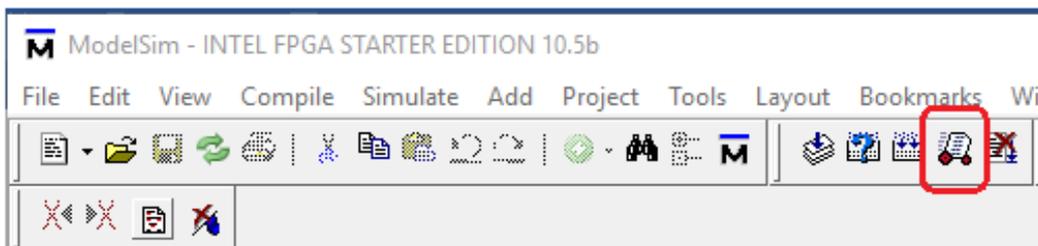
- נקבל



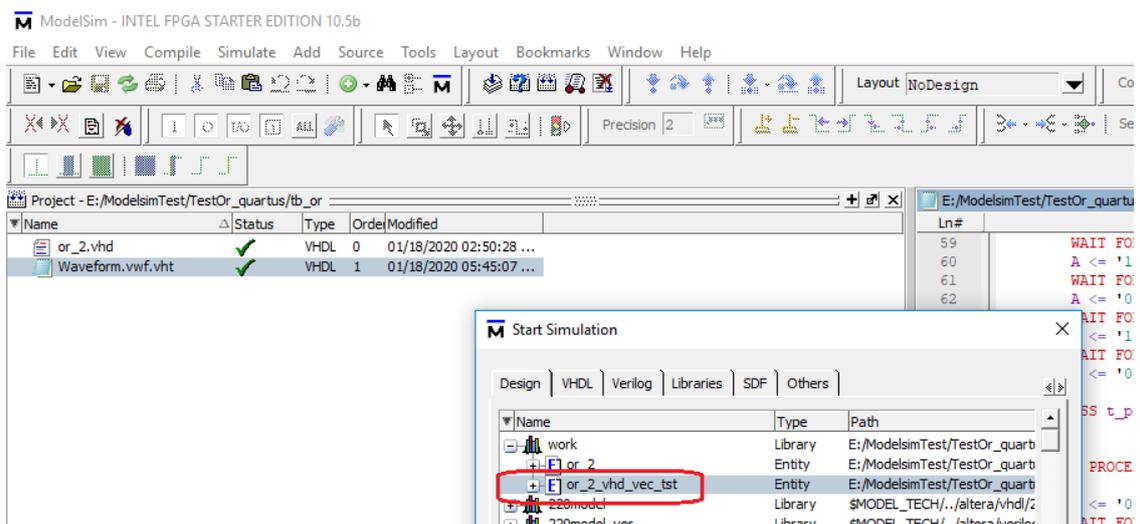
- נבצע קומפילציה לבדיקת תחביר הקבצים



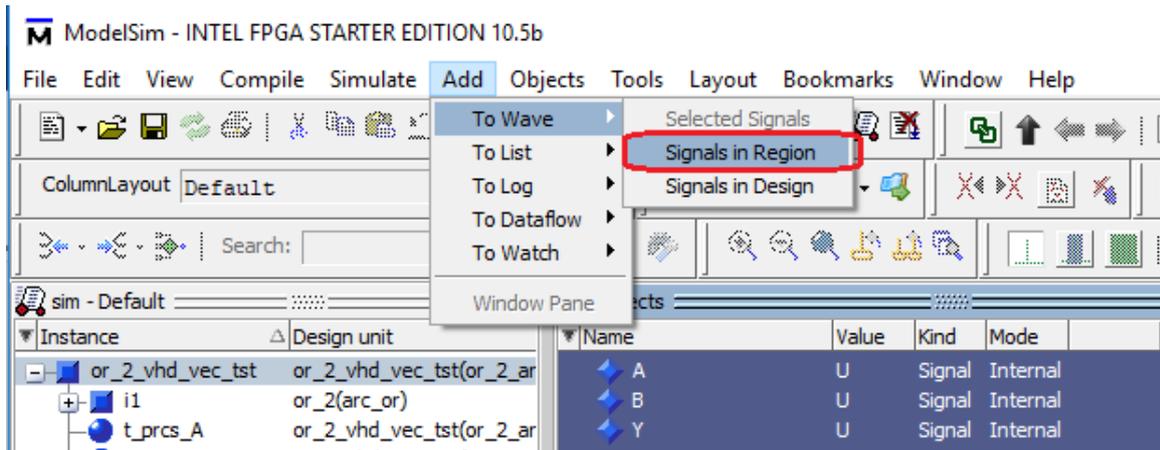
- נבחר simulate



- נבחר את קובץ בדיקה



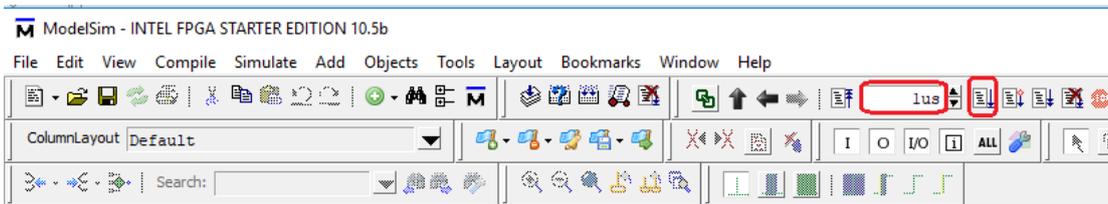
- מתוך מסך object נוסף את האותות השונים



- יפתח חלון



- נבחר זמן הרצה ונלחץ על פקד הרצה



- נריץ ונקבל

